IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of: Takeo Eguchi			
Application No:	10/790,986	Group Art Unit:	2193
Filed:	March 2, 2004	Examiner	Chat C. Do
Customer No.:	26263		
For:	SIGNAL PROCESSING AND ERROR ACCUMULATION REDUCING APPARATUS, STORAGE MEDIUM STORING THEREON COMPUTER READABLE CODES TO CONTROL THE SIGNAL PROCESSING AND ERROR ACCUMULATION REDUCING APPARATUS, AND SIGNAL		

Via EFS WEB ELECTRONIC FILING

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY BRIEF

Dear Sir:

In accordance with the provisions of 37 C.F.R. § 41.41(a)(1), Appellant submits herewith this Reply Brief in response to the Examiner's Answer mailed September 28, 2009. Appellant's arguments contained herein are intended to supplement Appellant's arguments contained within Appellant's Main Brief.

Please charge any deficiencies of fees associated with this communication to our deposit account no. 19-3140.

Respectfully submitted,

Dated: November 30, 2009

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STATUS OF CLAIMS

Claims 1-4 and 9-20 were pending and under consideration. The remaining claims, i.e., claims 5-8, were previously cancelled. A copy of claims 1-4 and 9-20 is appended hereto as the Claims Appendix.

The present Appeal is directed to claims 1-4 and 9-20, which were finally rejected under 35 U.S.C. § 103(a) in an Office Action dated November 24, 2008.

The status of the claims on appeal is as follows:

A) Claims 1-4, 9-13, and 17-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable in view of U.S. Patent No. 4,272,648 to Agrawal, et al. and U.S. Patent Publication No. 2001/0025292 to Denk, et al.

B) Claims 14-16 stand rejected under 35 U.S.C. §103(a) as being unpatentable in view of U.S. Patent No. 4,272,648 to Agrawal, et al., U.S. Patent Publication No. 2001/0025292 to Denk, et al. and Admitted Prior Art.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following grounds of rejection are to be reviewed on appeal:

A) Whether Claims 1-4, 9-13, and 17-20 are patentable under 35 U.S.C. §103(a) in view of U.S. Patent No. 4,272,648 to Agrawal, et al. and U.S. Patent Publication No. 2001/0025292 to Denk, et al.

B) Whether Claims 14-16 are patentable under 35 U.S.C. §103(a) in view of U.S. Patent No. 4,272,648 to Agrawal, et al., U.S. Patent Publication No. 2001/0025292 to Denk, et al. and Admitted Prior Art.

ARGUMENT

A. Claims 1-4, 9-13, and 17-20 are patentable over U.S. Patent No. 4,272,648 to Agrawal, et al. and U.S. Patent Publication No. 2001/0025292 to Denk, et al.

In the Examiner's Answer dated September 28, 2009 (hereinafter "Examiner's Answer"), the Examiner argues that the combination of Agrawal and Denk would not destroy the intended purpose of Agrawal, but would improve Agrawal's intended purpose by reducing/eliminating error during Agrawal's truncation or "chopping-off" process because rounding produces a smaller error than chopping off. *See* Examiner's Answer, pgs. 10-11. In attempt to demonstrate support for this argument, the Examiner observes that rounding and chopping-off an input of 5.39 respectively yields 5.3 with 0.09 error and 5.4 with 0.01 error. *See* Examiner's Answer, pg. 11. The Examiner's argument, however, is flawed for at least two reasons.

First, the Examiner neglects to consider Agrawal in its entirety and the intended purpose of Agrawal. Agrawal provides gain control while ensuring that each output signal is a close approximation to each input signal. *See* Agrawal, Abstract. Agrawal purports to accomplish this by chopping off an input and adding the chopped-off portion to a next output signal via a feedback loop, so that no portion of the input is ever lost. *See* Agrawal, Col. 7, Lns. 10-16, 65-68; Col. 8, Lns. 1-11. If one were to round input signals, it would be impossible to account for loss because the error produced during rounding disappears and a chopped-off portion is not produced. Thus, changing Agrawal from a chopping-off process to a rounding process would prevent Agrawal from executing its feedback loop, would prevent Agrawal from ensuring that each output signal is a close approximation to each input signal, and would destroy the intended purpose of Agrawal.

Second, the Examiner's example is deficient because it only illustrates an error generated from a single-round and fails to illustrate an error generated after multiple rounds, an error that would grow exponentially with each round. This is a significant deficiency because

Agrawal is not intended to be used only once, but is intended to be used repeatedly. If Agrawal were converted to a rounding process, use of Agrawal would generate in an enormous error over time. Agrawal avoids this problem by accounting for loss via the chopped-off portion, which is added to a next output signal so that no portion of an input is ever lost. In this manner, Agrawal ensures that each output signal is a close approximation to each input signal. Thus, it is unreasonable to suggest that one would convert Agrawal to a rounding process because doing such would not improve Agrawal.

In view of the foregoing additional arguments as well as the arguments previously submitted in Appellant's Main Brief, reversal of the Examiner's rejections as set forth in the final Office Action is requested.